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EXAMINER	
SILVER, DAVID	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/23/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/23/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/505,260	DALTON, DAMIAN	
	Examiner	Art Unit	
	David Silver	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 66-130 were originally presented for examination.

2. Claims 66-130 were rejected.

3. Claims 66-130 are currently pending in Instant Application.

4. The Instant Office Action is made in response to Remarks filed 1/19/2007 ("Remarks" or "Reply" hereinafter).

5. The Instant Application is not currently in condition for allowance.

Priority

6. Claimed priority has been acknowledged in previous Office Action.

10/505260 is a national stage entry of PCT/IS02/00023 filed **02/22/2002**.

Response to Arguments

Response: Information Disclosure Statement

7. **Background:**

"Applicant notes that the Information Disclosure Statement is not being considered because copies of the two references were not submitted." (Remarks: page 17)

8. **Applicant argues:**

8.1 "First, it is noted that these two references were cited in the International Search Report and accordingly copies of these references should be present in the Examiner's file.

8.2 Secondly, it is noted that the international application reference was cited by the Examiner in the PTO-892 form. Accordingly, Applicant submits that a copy of this reference is additionally unnecessary." (Remarks: page 17)

9. **Examiner Response:**

9.1 The Examiner was indeed able to retrieve the foreign patent document. However, the IDS still fails to comply because a copy of NPL (item CA**) was not supplied to the USPTO.

Response: Drawings

10. **Background:**

"The Examiner required a legend "Prior Art" be added to Figures 3, 8 and 10." (Remarks: page 17)

11. **Applicant argues:**

"By way of the present Amendment, Applicant has submitted replacement drawings including this legend." (Remarks: page 17)

12. **Examiner Response:**

Applicant is thanked for properly amending the drawings in response to the objection. The drawing objection has been withdrawn.

The drawings submitted on 1/29/2007 are acceptable.

Response: Claim Objections

13. Applicants are thanked for overcoming the claim objections set-forth in the Previous Office Action (7/27/06). The claim objections have been withdrawn.

Response: Claim Interpretation

14. **Background:**

"The Examiner states that reference to the use of the term "may" is not given patentable weight." (Remarks: page 18)

15. **Applicants argue:**

"By way of the present Amendment, Applicant has in many locations changed words "may", "if" and similar phrases in order that the phrases do not refer to intended use and accordingly should now be given patentable weight." (Remarks: page 18)

16. **Examiner Response:**

Applicant has, for example, changed "identifying segments that **may be** active" to "identifying segments that **are potentially** active". This again does not necessitate that the segments are active. All of the segments may be inactive. As such, bringing the 'potentially active' segments into associative memory does not produce a result because it is possible that no segments are active.

Response: 35 U.S.C. § 101

17. **Background:**

"Claims 66-84 and 97-130 stand rejected under 35 USC 101 as being directed to non-statutory subject matter, This rejection is respectfully traversed.

The Examiner points out that the method claims must produce a concrete, tangible and useful result. In regard to the apparatus claim, the Examiner states that the specification and claims demonstrate that the processor is not a tangible hardware element." (Remarks: page 18)

18. **Applicants argue:**

18.1 "Claim 66 has now been amended to recite the feature of "evaluating the active segments in the associative memory mechanism and storing the result of the evaluation." Applicant submits that information loaded into the associative memory mechanism is evaluated, thereby producing a concrete tangible, useful result that is stored Accordingly, Applicant submits that claim 66 as well as dependent claims 67-84 and 97-100 are directed to statutory subject matter." (Remarks: page 18)

18.2 "In regard to apparatus claims 101-130, Applicant submits that the processor is in fact tangible hardware element. The specific implementation recited in claim 130 is not the only possible implementation of that processor. In claim 130, the incorporated software code is used to program hardware to implement the processor while that code is being downloaded on a carrier wave. The carrier will itself be stored in a physical carrier such as a cable which constitutes a tangible hardware element. Other implementations of the processor are defined by other claims which may be implemented in other manners which are clearly structural." (Remarks: page 18)

19. **Examiner Response:**

19.1 Regarding subsection 1 *supra*, the storing does not produce a concrete useful and tangible final result in accordance with the MPEP. Specifically, in view of the "Response: Claim Interpretation" section above, the storing step may be storing the result of the evaluation of active segments. However, active segments are not necessitated by the claim language. As such, the storage step does not result in a concrete result. Furthermore, the Specification provide for storage in non-tangible medium. Thus, even if an active segment exists, the final result would not be tangible. Thus, claims 67-84 and 97-100 are drawn to non-statutory subject matter.

19.2 Regarding subsection 2 *supra*, Applicant is arguing limitations not claimed, such as, for example, "the carrier will itself be stored in a physical carrier such as a cable." Further, Applicant's attention is drawn to MPEP 2106, which recites, in part: "[A] claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected." Thus, the claims when given their broadest most reasonable interpretation consistent with the Specifications are drawn to non-statutory subject matter.

Response: 35 U.S.C. § 112 first and second paragraph

20. **Background:**

20.1 "The Examiner rejected claims 78 and 79 under 35 USC 112, first paragraph as failing to comply with the enablement requirement. The Examiner objected to the recitation of maximum state, the term S_0 and because they do not specify where the segment is brought." (Remarks: page 19)

20.2 "Claims 66-100, 116 and 129 stand rejected under 35 USC 112, first paragraph as being indefinite." (Remarks: page 19 – The Instant Claims were rejected under 35 USC 112 *second* paragraph as being indefinite. (emphasis added) This appears to be a minor oversight.)

21. **Applicants argue:**

21.1 "By way of the present Amendment, Applicant has amended these two claims in order to overcome these rejections. Applicant has corrected the term to refer to state S_0. Further, a description of the maximum state is provided in the specification between page 30, line 24 and page 32, line 7. The claims have further been modified to clarify that the segments are brought to the associative memory mechanism. Concerning the objection to the minimum state, Applicant does not see this phrase used in these claims."

21.2 "By way of the present Amendment, Applicant has amended these claims to provide proper antecedent basis. In addition, claim 66 has been amended to describe the term "external". Claim 78

has been amended to remove the ambiguity Claims 81 and 82 have been amended to delete phrase "in the normal manner'. Claim 89 has been amended to remove "appropriate" and "it". The term "most significant" has been deleted from claim 100." (Remarks: page 19)

22. **Examiner Response:**

22.1 Regarding subsection 1 *supra*, the 35 U.S.C. § 112 first and second paragraph rejections have been withdrawn in view of the appropriate amendments.

Response: 35 U.S.C. § 102

23. **Background:**

23.1 "Claims 66-68 and 101-103 stand rejected under 35 USC 102 as being anticipated by Dalton (An Associative Memory Approach to Parallel Logic Event-Driven Simulation)" (Remarks: page 19).

24. **Applicants argue:**

24.1 "[T]he present invention provides a method and processor that segments the circuit into manageable portions and therefore can handle circuits much larger than the method and processor described in Dalton. [...] Furthermore, contrary to the Examiner's view, Dalton does not disclose an external memory within the meaning of the Application in suit. By external memory, what is meant is additional memory other than the associative memory mechanism in which circuit segments and circuit information may be stored. [...] Dalton does not describe any such additional external memory Dalton stores an entire circuit in the associative memory mechanism. [...] The Examiner stated that it is inherent from Dalton that the circuit representation had to be stored in the external memory. However, Dalton clearly states that the circuit is stored in the associative memory mechanism. It is submitted that the meaning of external memory has been clarified in claims 66 and I01 and it is now clear and evident that this is not disclosed by Dalton. (Remarks: page 20-21)

24.2 "The "partitioning" described in Dalton which the Examiner appears to equate to the circuit segmentation of the Application in suit is in fact a description of the prior art methods of processing circuits which used a plurality of processors and is not in fact a method that was used in connection with an associative memory mechanism approach to parallel processing as described in the

remainder of the document by Dalton." (Remarks: page 20-21)

24.3 "Finally, the Applicant submits that Dalton does not assign a unique segment identifier to each segment within the meaning of the application in suit. Claim 66 and 101 have been amended to clarify this feature by reciting that "at least one of the circuit segments contains a plurality of logic gates"." (Remarks: page 20-21)

25. **Examiner Response:**

25.1 Regarding subsection 1 *supra*, the external memory is inherent to the disclosed system. Nevertheless in order to clarify the position previously taken, a 35 USC 103 rejection is presented below. A new rejection is presented below as necessitated by Applicant's amendments and remarks (that the external memory is external to the associated memory).

25.2 Regarding subsection 2 *supra,* Applicant's statement amounts to a merely conclusionary statement that partitioning is not the same as segmentation. In fact this amounts to, at best, a general allegation that the unclaimed intended use of the present invention is different than that of reference. Nevertheless, **(see 345 col 2 first full paragraph)**, which discloses "Tests [...] performed in parallel...".

25.3 Regarding subsection 3 *supra*, the unique identifiers are disclosed on **(page 345 col 1 last full paragraph: the host CPU would initialize the system by assigning gates to particular words)**. Specifically, the "particular words" are inherently unique because assigning a generic word would result in the gates being improperly identified. Meaning the look-up would result in unknown result, as such the "particular words" are unique such that the gates can be properly identified.

26. **Background:**

26.1 "Claims 66-130 stand rejected under 35 USC 102 as being anticipated by Dalton (WO 2001/01298). As indicated above, Applicant has added additional limitations to the independent claims which further help to define over this reference as well." (Remarks: page 22)

27. **Applicant argues:**

27.1 "Furthermore the method and processor according to the present invention allow for the circuit representation in external memory to be divided into a plurality of circuit segments, at least one of which contains a plurality of logic gates. By dividing the circuit up into a plurality of segments, it is possible to bring only those segments that are active in a particular' time sequence into the associative memory mechanism. This is not disclosed in WO 01/01298." (Remarks: page 22 – emphasis added by examiner)

27.2 "In addition to the above, according to the present invention, the method and processor may evaluate large circuits in a fast and efficient manner by bringing only those potentially active segments into the associative memory mechanism for evaluation and thereafter evaluating only those segments. Again this was not taught in Dalton which brought all of the gates in a circuit implementation into the associative memory mechanism and evaluated all of the gates simultaneously. In Dalton, tests were carried out on all gates and the results of the tests on all the gates were hand-picked for those gates that were required. Again this slowed down the processor." (Remarks: page 22)

27.3 "The Applicant also disagrees with the Examiner's assertion that WO 01/01298 disclosed a technique that allowed for dividing the circuit representation into a plurality of circuit segments WO 01/01298 mentions a prior art method of partitioning circuits when multiple processors are available as described in Breur et al but WO 01/01298 does not suggest using such a method in conjunction with associative memory mechanisms, as is the case with the present invention The disadvantages of such an approach were discussed, but nowhere did the Applicant of WO 01/01298 suggest providing circuit segments in the manner claimed in the present invention. Therefore, the Applicant respectfully submits that claims 66 mad I01 are novel in light of the disclosure WO 01/01298" (Remarks: page 22)

28. **Examiner Response:**

28.1 Regarding subsection 1 *supra*, Applicant is arguing that which is "possible" but not necessitated by the claim language. Specifically, the claims are broad enough to encompass bringing a while

circuit (in partitioned / segmented form – as disclosed in reference) into the associated memory. When a circuit is, for example, very simple and consists of elements that will be active at all times, the entire circuit is loaded into the associated memory.

28.2 Regarding subsection 2 and 3 *supra,* Applicant's statement amounts to a merely conclusionary statement that partitioning is not the same as segmentation. In fact this amounts to, at best, a general allegation that the unclaimed intended use of the present invention is different than that of reference. Nevertheless, the reference indeed teaches segmentation amongst associative memories **(page 60 lines 24-34)**.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:
Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

29. Claims 66-84 and 97-130 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

29.1 In this instance, absent an explicit and deliberate definition in the specification that the product includes an appropriate medium or hardware elements, the claims are directed to software, *per se.*

MPEP 2106 recites, in part:

"...USPTO personnel shall review the claim to determine it produces a useful, tangible, and concrete result. In making this determination, the focus is not on whether the steps taken to achieve a particular result are useful, tangible, and concrete, but rather on whether the *final* result achieved by the claimed invention is "useful, tangible, and concrete."

29.2 The method claims do not produce a useful, tangible, and concrete final result. The steps of the method claims do not produce a useful, tangible, and concrete result. They merely recite a software algorithm, per se, which, for example, does not display, store, or otherwise provide a useful tangible output.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

30. Claims 66-130 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Damian Dalton*** WO

01/01298 A2 ("Dalton").

Dalton discloses: 66. A parallel processing method of logic event simulation on circuits comprising a plurality of logic gates, the logic gates having interconnect lines therebetween, the method being carried out in a main processor and an associative memory mechanism, the associative memory mechanism comprising a plurality of associative arrays and at least one result register, characterized in that:

there is provided an external memory and means to transfer data between the associative memory and the external memory, external to the associative memory mechanism, the method comprising the steps of **(page 13 lines 25-28 - files)**:

storing a circuit representation in external memory **(page 28 "axyla.dat is the data file defining the gate and model types in the circuit")**;

dividing the circuit representation into a plurality of circuit segments, at least one of the circuit segments containing a plurality of logic gates **(page: 2 lines 15-18 and page 60 lines 28-30)**;

assigning a unique segment identifier to each segment **(page 8 line 8: "forming a unique word in the associative memory mechanism")**;

generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table **(pages: 16 line: 10-14; page 42 line 5: "Fan-out hdr table"; page 8 line 8)**;

for time period, identifying segments that are potentially active in that time period based on the segment data stored in the circuit segment table **(3 14-17; Fig 6 and texts which further expand on its features, page: 10 line: 27-28)**;

bringing only the potentially active segments into the associative memory mechanism from external memory for evaluation and evaluating the active segments in the associative memory mechanism and storing a result of the evaluation **(page 60 lines 24-34; this is an inherent feature of the disclosed reference)**.

Dalton discloses: 67. A parallel processing method of logic event simulation as claimed in claim 66 in which the segment data stored in the circuit segment table comprises the maximum delay state of a

segment, which indicates the maximum time delay in which any gate in the segment may make a transition **(page: 2 line: 4-6)**.

Dalton discloses: 68. A parallel processing method of logic event simulation as claimed in claim 66 in which the associative memory mechanism comprises a pair of associative arrays, associative array 1a and associative array 1b, an input value register bank and a hit list **(abstract, page: 1 line: 10-17)**.

Dalton discloses: 69. A parallel processing method of logic event simulation as claimed in claim 68 in which the circuit segment table data of associative array 1a, and associative array 1b and input value register bank are stored in external memory during segment evaluation **(page: 16 line: 15-26)**.

Dalton discloses: 70. A parallel processing method of logic event simulation as claimed in claim 66 in which after evaluation of a first segment the segment data of all the first segments fan-out gates are updated **(page: 16 line: 10-14, page: 20 line: 14-16: "fan-out gates are to be updated")**.

Dalton discloses: 71. A parallel processing method of logic event simulation as claimed in claim 70 in which when a new maximum delay state is greater than the previous maximum delay state of a fan-out segment, the segment data is updated with the new maximum delay state **(page: 20 line: 31-33: "The length of the delay word is ascertained and if the delay word width exceeds the associative.")**.

Dalton discloses: 72. A parallel processing method of logic event simulation as claimed in claim 66 in which inactive segments are not brought into the associative memory mechanism for evaluation until they have undergone an input change to a gate in that segment **(page: 4 line: 23-30, page 34 "If the current inspected bit is set, Hit_fndflag is asserted and the vector and the size (no. of gates) for the fan-out list loaded into Fan_out_src_reg and Fan_out_size_reg, respectively.")**.

Dalton discloses: 73. A parallel processing method of logic event simulation as claimed in claim 66 in which all interconnect lines are held in a segment dedicated to interconnect lines **(page: 11 line: 28-29)**.

Dalton discloses: 74. A parallel processing method of logic event simulation as claimed in claim 66 in

which all logic gates of a particular type are held in segments with logic gates of the same type **(page: 11 line: 1-5)**.

Dalton discloses: 75. A parallel processing method of logic event simulation as claimed in claim 68 in which the segment table is an N.sub.s.times.M bits segment table where N.sub.s is equal to the number of segments and M is equal to the sum of the number of bits wide of associative array 1a, associative array 1b, input value register and the hit list **(page: 10 line: 2, page: 6 line: 25-30, code allocating space on page 31)**.

Dalton discloses: 76. A parallel processing method of logic event simulation as claimed in claim 68 in which at least portion of associative array 1a, associative array 1b, input value register bank and the hit list are used to store the segment table at all times **(page: 10 line: 2: "input value register bank", page: 12 line: 8-9)**.

Dalton discloses: 77. A parallel processing method of logic event simulation as claimed in claim 68 in which when gate evaluations are completed for a particular time interval the previous segment table history is stored in the associative array 1b **(page: 11 line: 18-20, page: 10 line: 28-29, page: 55 line: 23-25, page: 4 line: 30-35, page: 5 line: 21-25)**.

Dalton discloses: 78. A parallel processing method of logic event simulation as claimed in claim 68 in which the input value register bank is shifted into associative array 1b **(page: 10 line: 10)**, and associative array 1a contains the maximum state of each segment, test patterns are then applied to contents of array 1b to determine transitions to lower states **(bottom of page 38: "These parameters define the upper and lower limits of the segments of the Group-test Hit list")**.

Dalton discloses: 79. A parallel processing method of logic event simulation as claimed in claim 66 in which segments in the state S.sub.O are brought in for evaluation **(bottom of page 38: "These parameters define the upper and lower limits of the segments of the Group-test Hit list")**.

Dalton discloses: 80. A parallel processing method of logic event simulation as claimed in claim 66 in which the minimum state of all segments, S.sub.STATEMIN, is calculated and all states are time advanced by S.sub.STATEMIN Time Units before evaluation of the segments commences **(bottom of**

page 38: "These parameters define the upper and lower limits of the segments of the Group-test Hit list").

Dalton discloses: 81. A parallel processing method of logic event simulation as claimed in claim 68 in which the set up time, T.sub.SETUP, of synchronous devices may be modelled where T.sub.setup=N.p+M, where N=integer, M=integer<P and P=bit width of array 1b, where by the following steps are performed:

the state entry of array 1a of a signal is set to S.sub.sn; a start marker is placed in the left most position of array 1b **(page: 21 line: 20-21)**;

array 1b is incremented in time and when start marker reaches the right-most position of array 1b and the signal has remained constant the state S.sub.sn is decremented to S.sub.sn-1, and the next time array 1b is incremented the start marker is returned to the left-most position in array 1b once again and array 1b is then incremented in the normal manner; the previous step is repeated until state entry S.sub.sn=S.sub.so, then the array 1b is incremented another M times **(page: 21 line: 20-21, page: 17 line: 28-29, page: 17 line: 19-25, page: 18 line: 10 - end of page)**; and

if the signal has remained constant for N.p+M time units then the state entry in array 1a is set to state setup, S.sub.SETUP **(page: 16 line: 5-7, page: 21 line: 30- page 22 line 10)**.

Dalton discloses: 82. A parallel processing method of logic event simulation as claimed in claim 68 in which the hold time, T.sub.HOLD, of synchronous devices may modelled where T.sub.hold=R.p+Q, and where R=integer, Q=integer<P and P=bit width of array 1b using the following steps:

when a clock makes a transition there is a search of state entries in array 1a to see if an input signal is in state S.sub.setup; any input signal in states in S.sub.setup are updated to the state S.sub.HR, and a start marker is placed in the left-most position of array 1b, array 1b is incremented and until the marker has made its way to the right-most position in array 1b and the signal has remained constant **(page: 21 line: 20-21)**;

the state is decremented to S.sub.HR-1, the start marker is returned to the left-most position in array 1b the next time that array 1b is incremented, array 1b is then incremented in the normal manner

and this is continued until the state is equal to S.sub.Ho,; when S.sub.HR=S.sub.HO then the array 1b is incremented a further Q times **(page: 21 line: 20-21, page: 17 line: 28-29, page: 17 line: 19-25, page: 18 line: 10 - end of page)**;

on the signal remaining constant over the entire period then the signal state is updated to S.sub.HOLD and the output value of the synchronous device is ascertained **(page: 16 line: 5-7, page: 21 line: 30- page 22 line 10)**.

Dalton discloses: 83. A parallel processing method of logic event simulation as claimed in claim 82 in which if the output value of the device has changed it is propagated to the fan-out list of the device **(page: 1 line: 5-20: "propagated to fan out gates")**.

Dalton discloses: 84. A parallel processing method of logic event simulation as claimed in claim 81 in which successive states are generated by causing a shift right operation in array 1a **(page: 17 line: 30-34: "process of updating the signal values of a particular wire is achieved by shifting right by one time unit all values")**.

Dalton discloses: 85. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided an amended result registering mechanism in which when a number of tests are carried out on a gate pair the result of each test is sent to a result register where on completion of all the tests the result register will indicate that all tests were successful or that at least one was unsuccessful **(page: 13 line: 19, page: 11 line: 10)**.

Dalton discloses: 86. A parallel processing method of logic event simulation as claimed in claim 85 in which the result register comprises an adder **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 87. A parallel processing method of logic event simulation as claimed in claim 85 in which the result register is a bi-state device **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 89. A parallel processing method of logic event simulation as claimed in claim 87 in which the result register on start-up is supplied with an appropriate priming input instead of last result so that it is ready to receive the first result **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 90. A parallel processing method of logic event simulation as claimed claim 85 in which

the amended result registering mechanism further comprises a result polarity circuit to invert a result and ensure a logic 1 is applied to the result register if the correct response to a test was for the test to be failed **(page: 13 line: 19)**.

Dalton discloses: 91. A parallel processing method of logic event simulation as claimed in claim 90 in which the result polarity circuit comprises a pair of AND gates, a pair of inverters and an OR gate, a result polarity control is fed to each of the AND gates, the other input of each of the AND gates being provided by the result of a test carried out on a gate pair, the inverters inverting the two inputs to one of the AND gates, the outputs of the AND gates being fed directly to the OR gate **(inherent in associative memory parallel searching, which is disclosed by the reference)**.

Dalton discloses: 92. A parallel processing method of logic event simulation as claimed in claim 85 in which the amended result registering mechanism is further provided with a logic combination circuit to determine whether an output gate pair of array 1b are ANDed or ORed together **(page: 18 line: 26-35)**.

Dalton discloses: 93. A parallel processing method of logic event simulation as claimed in claim 92 in which the logic combination circuit further comprises three AND gates and a logic combination circuit control, the logic combination circuit control being anded individually with each output of an array 1b gate pair and the gate pair anded in the third AND gate, when the logic combination requires an AND operation to be carried out, logic combination circuit control is given a value 0 and if an OR operation is required logic combination circuit control is given a logic value 1 **(inherent in associative memory parallel searching, disclosed by the reference)**.

Dalton discloses: 94. A parallel processing method of logic event simulation as claimed in claim 93 in which the logic combination circuit further comprises an OR gate, each of the outputs of the three AND gates being fed to the OR gate **(page: 18 line: 26-35; inherent)**.

Dalton discloses: 95. A parallel processing method of logic event simulation as claimed in claim 94 in which the output of the OR gate is led to the result polarity circuit as the result of a test carried out on a gate pair **(page: 18 line: 26-35; inherent)**.

Dalton discloses: 96. A parallel processing method of logic event simulation as claimed in claim 85 in which there is provided an amended result registering mechanism for each gate pair **(page: 11 line: 24-25)**.

Dalton discloses: 97. A parallel processing method of logic event simulation as claimed in claim 66 in which when all active segments have a state>S0, a check of all segment states is made until the lowest segment state S.sub.min is found, then each segment state is decremented by S.sub.min in order to advance simulation to the next evaluation stage **(page: 12 line: 4-6)**.

Dalton discloses: 98. A parallel processing method of logic event simulation as claimed in claim 97 in which the lowest state value is stored in a low global register each time there is a gate state change, if a new state is less than the lowest state value, the lowest state value in the low global register is replaced by the new state. **(page: 16 line: 1-8)**.

Dalton discloses: 99. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided a scan system comprising a priority decoder and a shift register **(page: 57 line: 10-15)**.

Dalton discloses: 100. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided a segment address table and the segment address table is divided into a number of rows, each row being M bits long, and each segment address is stored in the M-D bits of the segment row when the number of segments=2.sup.D **(inherent)**.

As per claims 101-126, note the rejection of claims 66-70, 73-75, 81-83, 85-90, 92-95, 97-99, 85, and 100 above, respectively. The Instant Claims are functionally equivalent to the above-rejected claims and are therefore rejected under same prior-art teachings.

Dalton discloses: 127. A processor as claimed in claim 101 in which the processor is embodied in computer readable format **(code on pages 28-54)**.

Dalton discloses: 128. A processor as claimed in claim 127 in which the processor in computer readable format may be stored on a disc **(page: 13 line: 27: file; code on pages 28-54)**.

Dalton discloses: 129. A processor as claimed in claim 127 in which the processor in computer readable

format may be stored on a record medium **(page: 13 line: 27: file; code on pages 28-54)**.

Dalton discloses: 130. A processor as claimed in claim 127 in which the processor in computer readable format may be stored on a carrier wave **(page: 13 line: 27: file; code on pages 28-54)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

31. Claims 66-68, and 101-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damian Dalton "An Associative Memory Approach to Parallel Logic Event-driven Simulation" ("Dalton"), and further in view of Official Notice taken.

Dalton discloses claim 66: A parallel processing method of logic event simulation on circuits comprising a plurality of logic gates, the logic gates having interconnect lines therebetween, the method being carried out in a main processor and an associative memory mechanism, the associative memory mechanism comprising a plurality of associative arrays and at least one result register **(abstract; page 344 annotation "register")**, characterized in that: dividing the circuit representation into a plurality of circuit segments, at least one of the circuit segments containing a plurality of logic gates **(page 341 col 2 annotated "partition")**; assigning a unique segment identifier to each segment **(page 344 and 345 annotation "unique id")**; generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table **(page 344 annotation "associated memory" and page 345 annotated "assoc. memory")**; for each time period, identifying segments that are potentially active in that time period based on the segment data stored in the circuit segment table **(page 345 annotated "ident. of active" and page 342 annotated "id. of**

active"); bringing only the potentially active segments into the associative memory mechanism from external memory for evaluation **(this is an inherent step in the disclosed reference)**; and evaluating the active segments in the associative memory mechanism and storing a result of the evaluation **(page 344 col 1 first paragraph; last sentence (item (ii)))**.

Dalton however does not expressly disclose there is provided an external memory and means to transfer data between the associative memory and the external memory, external to the associative memory mechanism, the method comprising the above mentioned steps and storing a circuit representation in external memory. Official Notice is taken with respect to this limitation. Specifically, Dalton discusses the use of circuit models and the simulation thereof. Circuit models can range from very simple to very complex. When the circuit models are complex it is unrealistic and at times impossible to manually input the models each time a simulation is performed. Therefore, external memory (external storage) is used. Such external memory can be, for example, a harddrive and a file thereon which contain the model. It would have been obvious to one of ordinary skill in the art to combine the features in order to create a faster simulation by not having to manually re-generate the circuit model each time a simulation is performed, and by using an already-made circuit model. Thus, saving the time and money associated with regenerating the circuit model by saving it to an external memory element (such as a harddisk drive).

Dalton discloses: 67. A parallel processing method of logic event simulation as claimed in claim 66 in which the segment data stored in the circuit segment table comprises the maximum delay state of a segment, which indicates the maximum time delay in which any gate in the segment may make a transition **(page 342 annotations "item predefined units of time" and "delay models"; page 343 annotation "delay models")**.

Dalton discloses: 68. A parallel processing method of logic event simulation as claimed in claim 66 in which the associative memory mechanism comprises a pair of associative arrays, associative array 1a and associative array 1b, an input value register bank and a hit list **(page 344 annotation "associative memory"; page 345 "assoc. memory" and "hit list")**.

As per claim(s) 101-103, note the rejection of claim(s) 66-68 above. The Instant Claim(s) is/are functionally equivalent to the above-rejected claim(s) and is/are therefore rejected under same prior-art teachings.

Conclusion

32. All claims are rejected.

33. The Instant Application is not currently in condition for allowance.

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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